What is claimed is:

1. A semiconductor device comprising:

an insulating film formed over a semiconductor substrate;

an adhesive layer formed on the insulating film;

a capacitor lower electrode formed on the adhesive layer;

a ferroelectric layer formed on the capacitor lower electrode, and having an ABO_3 perovskite structure that contains Ir in at least one of an A site and a B site (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr); and

a capacitor upper electrode formed on the ferroelectric layer.

2. A semiconductor device according to claim 1, wherein a (111) orientation of the ferroelectric layer has an inclination of 3.5 ° or less from a perpendicular direction of an upper surface of the semiconductor substrate.

3. A semiconductor device according to claim 1, wherein the ferroelectric layer is material that has PZT as a main component.

4. A semiconductor device according to claim 1, wherein a (111) orientation of the lower electrode has an inclination of 2.3 ° or less from the perpendicular direction of the upper surface of the semiconductor

substrate.

5. A semiconductor device according to claim 1, wherein the lower electrode is made of platinum.

6. A semiconductor device according to claim 1, wherein roughness of an upper surface of the adhesive layer is 0.79 nm or less.

7. A semiconductor device according to claim 1, wherein the adhesive layer is made of alumina.

8. A semiconductor device according to claim 1, wherein the upper electrode is made of iridium oxide or iridium.

9. A semiconductor device comprising:

an insulating film formed over a semiconductor substrate;

an adhesive layer formed on the insulating film and having a surface roughness of 0.79 nm or less;

a capacitor lower electrode formed on the adhesive layer, and having a (111) orientation that is inclined from a perpendicular direction of an upper surface of the semiconductor substrate by 2.3 ° or less;

a ferroelectric layer formed on the capacitor lower electrode, and having an ABO_3 perovskite structure (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr); and

a capacitor upper electrode formed on the ferroelectric layer.

10. A semiconductor device according to claim 9, wherein a (111) orientation of the ferroelectric layer is inclined from a perpendicular direction of an upper surface of the semiconductor substrate by 3.5 ° or less.

11. A semiconductor device comprising:

an insulating film formed over a semiconductor substrate;

an adhesive layer formed on the insulating film;

a capacitor lower electrode formed on the adhesive layer;

a ferroelectric layer formed on the capacitor lower electrode, and having a (111) orientation that is inclined from a perpendicular direction of an upper surface of the semiconductor substrate by 3.5 ° or less, and having an ABO_3 perovskite structure (A=any onf of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any one of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr); and

a capacitor upper electrode formed on the ferroelectric layer.

12. A semiconductor device according to claim 9, wherein the lower electrode is made of any one of a platinum layer, an iridium layer, a platinum- containing layer, and an iridium-containing layer.

13. A semiconductor device according to claim 9, wherein the ferroelectric layer is made of material that contains PZT as a main component, or PZT.

14. A semiconductor device according to claim 9,

further comprising:

a hole formed in the insulating film and the adhesive layer under the lower electrode; and

a conductive plug formed in the hole and connected to the lower electrode.

15. A semiconductor device according to claim 14, wherein an oxygen barrier metal layer is formed between the conductive plug and the lower electrode.

16. A semiconductor device according to claim 15, wherein the oxygen barrier metal layer constitutes a part of the lower electrode.

17. A manufacturing method of a semiconductor device comprising the steps of:

forming an insulating film over a semiconductor substrate;

forming an adhesive layer, whose surface roughness is 0.79 nm or less, on the insulating film;

forming a first conductive film, whose (111) orientation is inclined from a perpendicular direction of an upper surface of the semiconductor substrate by 2.3 ° or less, on the adhesive layer;

forming a ferroelectric layer on the first conductive film;

forming a second conductive film on the ferroelectric layer;

forming a capacitor upper electrode by patterning the second conductive film;

leaving the ferroelectric layer at least under the upper electrode by patterning the ferroelectric layer; and

forming a capacitor lower electrode below the upper electrode by patterning the first conductive film.

18. A manufacturing method of a semiconductor device according to claim 17, wherein the ferroelectric layer is formed by any growing method of a sputter, a MOCVD, a spin-on method using an MOD solution, and a spin-on method using a sol-gel solution.

19. A manufacturing method of a semiconductor device comprising the steps of:

forming an insulating film over a semiconductor substrate;

forming an adhesive layer on the insulating film;

forming a first conductive film on the adhesive layer;

forming a ferroelectric layer, which has an ABO_3 perovskite structure that contains an Ir element in at least one of an A site and a B site (A=any one of Bi, Pb, Ba, Sr, Ca, Na, K, and a rare earth element, B=any of Ti, Zr, Nb, Ta, W, Mn, Fe, Co, and Cr), on the first conductive film;

forming a second conductive film on the ferroelectric layer;

forming a capacitor upper electrode by patterning the second conductive film;

leaving the ferroelectric layer at least under the upper electrode by patterning the ferroelectric layer; and

forming a capacitor lower electrode below the upper electrode by patterning the first conductive film.

20. A manufacturing method of a semiconductor device according to claim 19, wherein the ferroelectric layer is formed by any one of a MOCVD using an organic source containing Ir, a sputter using a target containing Ir, and a spin-on method using a sol-gel solution having the Ir element or an MOD solution having Ir.

21. A manufacturing method of a semiconductor device according to claim 19, wherein the step of forming the ferroelectric layer includes the steps of,

forming a ferroelectric material layer,

forming the second conductive film, which is made of any one of iridium and iridium-containing material, on the ferroelectric material layer, and

doping Ir from the second conductive film into the ferroelectric material layer by heat.

22. A manufacturing method of a semiconductor device according to claim 17, further comprising the step of:

heating the ferroelectric layer before formation of the second conductive film; and

heating the second conductive film and the ferroelectric layer.

23. A manufacturing method of a semiconductor device according to claim 17, wherein a platinum film is formed as the lower electrode.

24. A manufacturing method of a semiconductor device comprising the steps of:

forming an insulating film over a semiconductor substrate;

forming an adhesive layer, whose surface roughness is 0.79 nm or less, on the insulating film;

forming a first conductive film, which is made of either iridium or iridium-containing material, on the adhesive layer;

forming a ferroelectric layer, which contains 90 % or more of grains with a (111) orientation on an upper surface side, on the first conductive film by a MOCVD growth method;

forming a second conductive film on the ferroelectric layer;

forming a capacitor upper electrode by patterning the second conductive film;

leaving the ferroelectric layer at least under the upper electrode by patterning the ferroelectric layer; and

forming a capacitor lower electrode below the upper electrode by patterning the first conductive film.

25. A manufacturing method of a semiconductor device according to claim 18, wherein a growth

temperature of the ferroelectric layer when the ferroelectric layer is formed by the MOCVD is set between 600 to 650 ℃.

26. A manufacturing method of a semiconductor device according to claim 17, wherein the (111) orientation of the ferroelectric layer is set to an inclination of 3.5 ° or less from a perpendicular direction of an upper surface of the semiconductor substrate at a time of growth or by an annealing process.

27. A manufacturing method of a semiconductor device according to claim 17, wherein the ferroelectric layer is made of material containing PZT as a main component or PZT.

28. A manufacturing method of a semiconductor device according to claim 17, wherein an alumina is formed as the adhesive layer.

29. A manufacturing method of a semiconductor device according to claim 28, wherein the alumina is formed while setting a temperature of the semiconductor substrate to 100 ℃ or less.

30. A manufacturing method of a semiconductor device according to claim 19, wherein the lower electrode is formed under a condition that a (111) orientation is set to incline from a perpendicular direction of an upper surface of the semiconductor substrate by 2.3 ° or less.

31. A manufacturing method of a semiconductor device according to claim 17, further comprising the

steps of:

forming a hole in the insulating film and the adhesive layer under the capacitor lower electrode; and

forming a conductive plug, which is connected to the capacitor lower electrode, in the hole.

32. A manufacturing method of a semiconductor device according to claim 31, wherein an oxygen barrier metal layer is formed between the conductive plug and the capacitor lower electrode.